REMARKS

Claims 1-15 are currently pending. By this amendment, claims 1-10 are amended for the Examiner's consideration. Support for the amendment is provided in at least Figure 3, and at pages 5-11 of the present specification. Claims 1-10 are not amended for reasons of patentability and are not to be construed as narrowing amendments. These claim amendments are made to better comport with U.S. patent prosecution guidelines. No new matter is added. Reconsideration of the rejected claims in view of the above amendment and the following remarks is respectfully requested.

35 U.S.C. §102 Rejection

Claims 1 and 11 are rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,434,590 issued to Blelloch, *et al.* ("Blelloch"). This rejection is respectfully traversed.

In embodiments, individual processors or task units may be dedicated to particular tasks or operations. A task interconnection logic interconnects the task units for communicating actions from a source task unit to a destination task unit. A processor included in each task unit executes the steps of the associated task in response to a received request action and runs the steps of the actions received from other task units. A status manager in each task unit is connected to the processor. The status manager means handles actions from source task units and builds actions to be sent to destination task units.

In particular, the task interconnection logic receives a task or action from the status manager of a task or action from the status manager of a task unit and analyzes at least a portion of the task to determine the appropriate destination task unit. Consequently, each task unit may be configured to repeatedly run only a particular task. Use of the task interconnection guarantees that any particular task unit receives only those tasks for which it is configured to run.

The actions are built using a data field and a control field of the current task together with the contents of a first configuration register and a second configuration register. Information, in the form of bits, contained in the control and data fields causes the status manager to load data into the processor, which then processes the data. When processing is complete, the processor passes a complete signal back to the status manager. The status manager receives the processed task, which includes new data in the control and data fields, and builds an action (command) using the new data and the configuration registers. Once complete, the command is forwarded to another task unit.

In contrast, Blelloch does not show all the features of the claimed invention. In fact, after careful review, it is clear that Blelloch does not teach at least the status manager as recited in the invention. For example, Blelloch shows, in Figures 2, 2a, and 3, providing a single assignment manager to a plurality of processing elements. The assignment manager supplies a set of available tasks and makes them available to each processing element. This directly contradicts the claimed invention, claim 1 of which recites, in part:

> "each of said task units including a ... a status manager for handling actions from source task omits and building actions to be sent to destination units."

Clearly, the assignment manager in Blelloch is not the status manager or equivalent as in the claimed invention because Blelloch specifically teaches that its processing units do not include status managers. In fact, the examiner admitted as such at page 4 of the Office Action, which states:

> Blelloch taught to use one status manager in associating with the task units in the processing system (col. 2, lines 43-60) where the status manager receive actions from the interconnection logic means and directing execution of the single task (col. 2, lines 52-55). Blelloch did not specifically teach at least two status managers each being associated with each of the at least two task units, respectively.

Consequently claim 1 is an allowable condition. Additionally, claim 11 is also allowable for at least the reasons set forth with respect to claim 1, from which it depends, as well as for its added features. Applicants respectfully request that the rejection of claims 1 and 11 be withdrawn.

35 U.S.C. §103 Rejection

Claims 2-3 and 12-15 were rejected under 35 U.S.C. §103(a) for being unpatentable over Blelloch in view of Official Notice. Claim 4 was rejected under 35 U.S.C. § 103(a) for being unpatentable over Blelloch and U.S. Patent No. 5,430,850 to Papadopoulos, *et al.* ("Papadopoulos"). Claims 5-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Blolloch in view of Papadopoulos and Official Notice. Claim 10 was rejected under 35 U.S.C. §103(a) for being unpatentable over Blelloch in view of Papadopolous and in view of

U.S. Patent No. 5,321,842 to Fairfield, *et al.* ("Fairfield"). These rejections are respectfully traversed.

I. Official Notice

Documentation is typically required to support Official Notice: "Ordinarily, there must be some form of evidence in the record to support an assertion of common knowledge. *In re Lee*, 277 F.3d 1338, 1344-45, 61 USPQ2d 1430, 1434-35 (Fed. Cir. 2002)." MPEP 2144.03(B). Undocumented Official Notice must include specific factual support: "The examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge. *In re Soli*, 317 F.2d 941, 946, 137 USPQ 797, 801 (CCPA 1943)." *Id.* Official Notice may be traversed by pointing out errors in the examiner's action, including why the fact is not common knowledge. 37 C.F.R. 1.111(b); MPEP 2144.03(C). If Official Notice is adequately traversed by the applicant, the examiner must provide appropriate documentation or withdraw the Official Notice. 37 C.F.R. 1.104(c)(2); MPEP at *id.*

Regarding claim 2, the Examiner notes that Blelloch does not specifically teach the actions to include KILL used to cancel the task associated with the destination task unit. The Examiner then takes undocumented Official Notice that it would been obvious to implement Blelloch's system with commands such as KILL and PAUSE to perform administrative actions. Applicants traverse the undocumented Official Notice, and note that no factual basis is provided to support the assertion that it is common knowledge that administrative commands which

function in system of one particular design would properly function in a second system of a different particular design. Accordingly, Applicants respectfully traverse the Examiner's assertion that it would have been obvious to add different commands to perform desired actions according to administrating needs (e.g., well known in the art). Pursuant to M.P.E.P. §2144.03 Applicants request that the Examiner (i) withdraw the rejection or (ii) supply evidence, e.g., a prior art reference, supporting the asserted "well known" feature. If the rejection is not withdrawn, Applicants request the Examiner to provide a factual basis for documentation indicating that the Blelloch system would properly function using the KILL and PAUSE commands as defined in Applicants' specification.

Further regarding claims 2 and 3, Applicants submit that these claims depend from claim 1, and are allowable over Blelloch for at least the reasons set forth with respect to claim 1, as well as for their added features. Accordingly, Applicants request that the rejection of claims 2-3 be withdrawn.

Regarding claim 12, the Examiner notes that:

> "Blelloch did not specifically teach at least two status managers each being associated with each of the at least two task units, respectively."

However, the Examiner then takes undocumented Official Notice that it would have been obvious:

> "to eliminate the need of having more than one status manager and lower the cost of the device since the one status manager taught in Blelloch's device is able to

> perform the same desired needs of having multiple status manager."

Applicants traverse the undocumented Official Notice, and note that no factual basis is provided to support the Examiner's broad assertion, which is factually incorrect. Also, contrary to the Examiner's statement, the claimed invention does not "eliminate the need of having more than one status manager..." In fact, the exact opposite is true: the claimed invention, in direct contrast to the teachings of Blelloch, specifically recites a status manager in each task unit. This provides the advantage of being able to process multiple tasks simultaneously without a single processor receiving all the tasks. Accordingly, Applicants submit that claim 12 is allowable. Claims 13-15 depend from claim 12 and are allowable for at least the reasons discussed with respect to claim 12, as well as for their added features. Therefore, Applicants request that the rejection of claims 12-15 be withdrawn.

II. Claims 4-10

A §103 rejection requires the Examiner to first establish a prima facie case of obviousness: "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness." M.P.E.P. § 2142. The Court of Appeals for the Federal Circuit has set forth three elements which must be shown for prima facie obviousness:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

As discussed in Applicants' previous response, Papadopoulos teaches away from the claimed invention. For example, Papadopoulos teaches routing the entire code or algorithm to every processing unit. This directly contrasts with the claimed invention which runs only portions of the entire code or algorithm on individual processing units. Papadopoulos permits each processor run any task when the necessary data arrives at that processor. The present invention, by contrast does not permit this, but rather assigns certain processors to certain tasks. Moreover, as previously discussed, the synchronization coprocessor and Rmem processor taught by Papadopoulos are not the task interconnection logic and source task units recited by the claimed invention.

Regarding claim 4, the Examiner notes that Blelloch does not teach that the status manager is a state machine. The Examiner then asserts that Papadopoulos teaches a status manager that is a state machine. However, this assertion appears to be incorrect. At Col. 26, lines 54-60, Papadopoulos discloses a Rmem processor which receives messages destined for a current node, and either sends a message back to the requesting processor or elicits a trap on the current processor for handling conditions beyond its capability. Because the Rmem processor

only communicates with a source processor or its own processor, and does not handle actions from multiple source task units or build actions to be sent to multiple destination task units, it is not a status manager, as recited by the invention.

As to the Examiner's specific remarks regarding claim 4, it was suggested that it would have been obvious for one skilled in the art to combine the teachings of Papadopoulos and Blelloch because Papadopoulos' status manager enables the status manager in Blelloch's device to consume messaging abilities. Applicants respectfully traverse this suggestion on the grounds that neither Papadopoulos nor Blelloch, for the reasons stated above, disclose the status manager as claimed. This is based on: (i) the Rmem processor taught by Papadopoulos only communicates with itself and another processor, (ii) the assignment manager of Blelloch communicates with a plurality of processing units, and (iii) the Rmem processor and assignment manager each perform entirely different functions. For these reasons, Applicants respectfully request that the rejection of claim 4 be withdrawn.

Regarding the rejection of claims 5-9, Applicants note that these claims depend from claim 1 and are allowable over Blelloch and Papadopoulos for at least the reasons stated with respect to claim 1, as well as for their added features. Regarding the Official Notice taken by the Examiner with respect to each of claims 5-9, Applicants note that no specific factual basis was provided as required by the MPEP and case law. Accordingly, Applicants traverse the Examiner's assertions that the features of claims 6-9, in combination with the independent base claim,

1. would have been obvious to load a data field or execute any info when an action is received (claim 6);

2. would have been obvious to send a completion bit to the status manager in Blelloch and Papadopoulos' systems to notify the completion of task execution in the system (claim 7);

3. would have been obvious to one of ordinary skill in the art to use a kill action in Blelloch and Papadopoulos' systems to clear a specific instance (claim 8); and

4. would have been obvious to use CONFIG.L and CONFIG.R in Blelloch and Papadopoulos' system (claim 9).

Pursuant to MPEP 2144.03 and with regard to the reasons stated above with respect to claims 1-4, Applicants request the Examiner to (i) withdraw the rejection of claims 5-9 or (ii) provide references which show these features.

Regarding claim 10, the Examiner again suggests that it would be obvious to employ a three state driver taught by Fairfield to provide feedback to the processor in Papadopoulos and Blelloch's systems. Applicants traverse this rejection and respectfully submit that the Examiner's assertion is not correct. Claim 10 recites, in part:

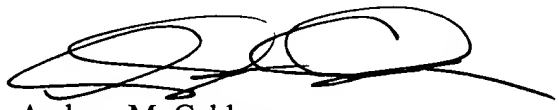
> "... three state drivers, each one of said drivers being associated with one of said tasks as an input task and a number of bases equal to the number of said tasks as output tasks..."

On the other hand, Fairfield specifically teaches using a three state driver connected to a single bus to prevent interference between processors accessing a single memory through a shared bus. This teaching directly contradicts the claimed invention in which each driver is "associated with an input task and a number of buses equal to the number of said tasks." Moreover, Fairfield does not teach other features of the claimed invention, such as, but not limited to, the status managers associated with each task unit. Thus, even if the teachings of Blelloch, Papadopoulos and Fairfield were combined, the resultant combination would not disclose each feature of the claimed invention. For these reasons, the Examiner has not established a prima facie case of obviousness, and Applicants request that the rejection of claim 10 be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to IBM Deposit Account No. 09-0457.

Respectfully submitted,



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